

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111
Serial Number: 09/726,629
Filing Date: November 30, 2000
Title: SOLDERLESS ELECTRONICS PACKAGING (as amended)
Assignee: Intel Corporation

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Dkt: 884.341US1 (INTEL)

IN THE SPECIFICATION

Please make the paragraph substitutions indicated below. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs.

The sub-title on page 1, line 6 is amended as follows: Technical Field ~~of the Invention~~

The paragraph beginning on page 1, line 8 is amended as follows:

a1
The inventive subject matter ~~present invention~~ relates generally to electronics packaging. More particularly, the inventive subject matter ~~present invention~~ relates to an electronic package that includes an integrated circuit package or an integrated circuit coupled to a substrate with a solderless compression connector, and to manufacturing methods related thereto.

a2
The sub-title on page 1, line 13 is amended as follows: Background Information ~~of the Invention~~

The sub-title on page 5, line 5 is amended as follows: Detailed Description ~~of Embodiments of the Invention~~

The paragraph beginning on page 5, line 7 is amended as follows:

a3
In the following detailed description of embodiments of the inventive subject matter ~~invention~~, reference is made to the accompanying drawings which form a part hereof, and in which are ~~are~~ ~~shown~~ by way of illustration specific preferred embodiments in which the inventive subject matter ~~inventions~~ may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the inventive subject matter ~~invention~~, and it is to be understood that other embodiments may be utilized and that mechanical, chemical, electrical, and procedural changes may be made without departing from the spirit and scope of the inventive subject matter ~~present invention~~. Such embodiments of the inventive subject matter may be referred to, individually and/or collectively, herein by the term "invention" merely for convenience and without intending to voluntarily limit the scope of this

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Q3
application to any single invention or inventive concept if more than one is in fact disclosed.

The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of embodiments of the present invention is defined only by the appended claims.

The paragraph beginning at page 6, line 10 is amended as follows:

Q4
FIG. 1 is a block diagram of an electronic system 1 incorporating at least one solderless electronic assembly 4 with a reduced thickness or stack height in accordance with one embodiment of the invention. Electronic system 1 is merely one example of an electronic system in which embodiments of the present invention can be used. In this example, electronic system 1 comprises a data processing system that includes a system bus 2 to couple the various components of the system. System bus 2 provides communications links among the various components of the electronic system 1 and can be implemented as a single bus, as a combination of busses, or in any other suitable manner.

The paragraph beginning at page 8, line 28 is amended as follows:

Q5
As mentioned earlier, the inventive subject matter ~~present invention~~ provides a solution to package socketability and thickness limitations and to loop induction problems that are associated with prior art packaging of integrated circuits that operate at high clock speeds and high power levels by eliminating any solder interconnect between an IC die and an IC package substrate and/or between an IC package and a PCB. In the ensuing description, the use of a solderless connector in an IC package will first be described, and then the use of a solderless connector in coupling an IC package to a substrate such as a PCB will be described. Finally, an embodiment that employs solderless connectors at two different packaging levels, i.e. both within the IC package and in mounting the IC package to a PCB, will be described.

The paragraph beginning at page 10, line 17 is amended as follows:

Q6
Connector 120 can be a modified version of an electrical connection system known under the trade name CIN::APSE and commercially available from Cinch Connectors, Lombard, Illinois, U.S.A. Product information on the CIN::APSE interconnect technology is currently obtainable from the Internet at a URL that includes "cinch.com/products"

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<http://www.cinch.com/products> (To avoid inadvertent hyperlinks, the "http://www" has been omitted from the foregoing URL.)

The paragraph beginning at page 10, line 22 is amended as follows:

27
The known CIN::APSE connection system differs in several significant respects from connector 120. First, the CIN::APSE connection system incorporates a socket fixture on the order of several millimeters in thickness between the IC die and the substrate. By contrast, the inventive subject matter present invention does not incorporate a socket fixture, so the thickness of support 121 of connector 120 can range from a few tenths of a millimeter down to .05 mm and possibly thinner.

The paragraph beginning at page 15, line 22 is amended as follows:

28
Substrate 140 can be of any type, such as a printed circuit board (PCB) or card, a motherboard, or any other type of packaging element. Substrate 140 can be a multi-layered substrate or a single-layered substrate. Embodiments of the inventive subject matter are The ~~present invention~~ is not to be construed as limited to any particular type of substrate 140 or to any particular method of coupling IC package 105 (FIG. 8) to substrate 140. Substrate 140 can optionally have lands 146 on its lower surface for attachment to an additional substrate or other packaging structure.

Please delete the sub-title "Conclusion" on page 21, line 1.

The paragraph beginning at page 21, line 4 is amended as follows:

29
The inventive subject matter present invention provides for a socketable electronic package, in several different embodiments, and for methods of manufacture thereof, that minimize the thickness of the package and that minimize loop inductance within the package. An electronic system and/or data processing system that incorporates one or more electronic assemblies that utilize the inventive subject matter present invention can be produced in configurations having socketable IC's and/or IC packages, with reduced physical dimensions,

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A⁹ and with enhanced electronic performance, and such systems are therefore more commercially attractive.

The paragraph beginning at page 21, line 12 is amended as follows:

A¹⁰ As shown herein, the inventive subject matter ~~present invention~~ can be implemented in a number of different embodiments, including an electronic package, an electronic assembly, an electronic system, a data processing system, methods for packaging an IC, and methods for mounting an IC package on a substrate. Other embodiments will be readily apparent to those of ordinary skill in the art. The elements, materials, geometries, dimensions, and sequence of operations can all be varied to suit particular packaging requirements.

The paragraph beginning at page 21, line 19 is amended as follows:

A¹¹ For example, while an embodiment of an IC is shown in which signal traces are provided around the periphery and in which power supply traces are provided at the die core, the inventive subject matter ~~invention~~ is equally applicable to embodiments where signal traces and power supply traces are provided anywhere on the die.

The paragraph beginning at page 21, line 23 is amended as follows:

A¹² Further, embodiments of the inventive subject matter ~~are the present invention~~ is not to be construed as limited to use in land grid array (LGA) packages, and they ~~it~~ can be used with any other type of IC package where the herein-described features of the inventive subject matter ~~present invention~~ provide an advantage.

The paragraph beginning at page 22, line 1 is amended as follows:

A¹³ While a ball grid array (BGA) arrangement 56 is illustrated in FIG. 15 for coupling IC package 105 (FIG. 8) to substrate 140 (FIG. 15), embodiments of the inventive subject matter ~~are the present invention~~ is not limited to use with a BGA arrangement, and they ~~it~~ can be used with any other type of packaging technology, e.g. land grid array (LGA), chip scale package (CSP), or the like.

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The paragraph beginning at page 22, line 13 is amended as follows:

A14
The particular implementation of the inventive subject matter invention is very flexible in terms of the orientation, size, number, and composition of its constituent elements. Various embodiments of the invention can be implemented using various combinations of thin film and ACF technology, particle and wire wad technology, substrate technology, and IHS technology to achieve the advantages of the inventive subject matter present invention.

The paragraph beginning at page 22, line 18 is amended as follows:

A15
FIGS. 1 through 17 are merely representational and are not drawn to scale. Certain proportions thereof may be exaggerated, while others may be minimized. FIGS. 1 and 5-19 are intended to illustrate various implementations of the inventive subject matter invention that can be understood and appropriately carried out by those of ordinary skill in the art.

The paragraph beginning at page 22, line 23 is amended as follows:

A16
Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the inventive subject matter present invention. Therefore, it is manifestly intended that embodiments of this invention be limited only by the claims and the equivalents thereof.